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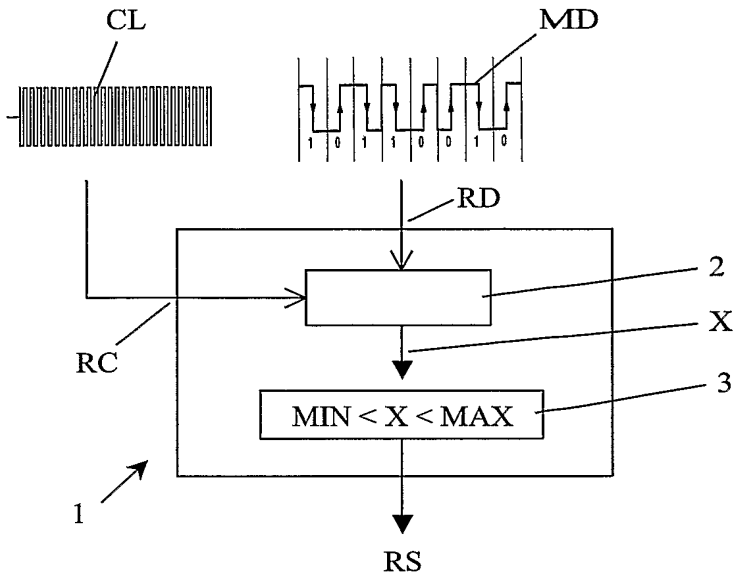
(54) Title: RESET CIRCUIT, DATA CARRIER AND COMMUNICATION DEVICE



(57) Abstract: In a reset circuit (1) comprising a clock signal input (RC) for receiving a clock signal (CL) consisting of a sequence of clock signal cycles, and comprising a data signal input (RD) for receiving digital data signals (MD), which are encoded in such a manner that at least one signal edge (0→1, 1→ 0) appears per data bit in the data signal, are provided a counter (2) being connected to the data signal input (RD) and the clock signal input (RC) and being designed for counting the number (X) of clock signal cycles, which appear between a defined number of data signal edges, and comparing means (3), which comparing means (3) being designed for comparing the number (X) of clock signal cycles counted by the counter (2) with a lower limit (MIN) and/or with an upper limit (MAX) and which comparing means (3) being designed to produce a reset signal (RS), if the number (X) either remains below the lower object (MIN) or exceeds the upper limit (MAX), depending on the limit value (MIN, MAX) taken for comparison.

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